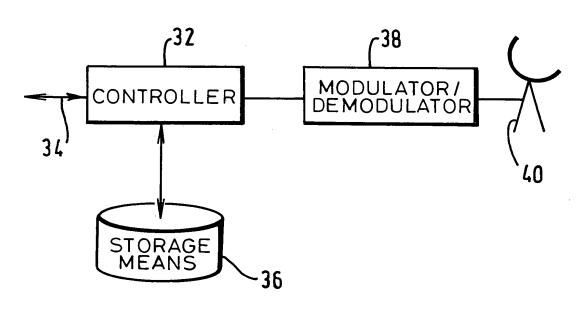
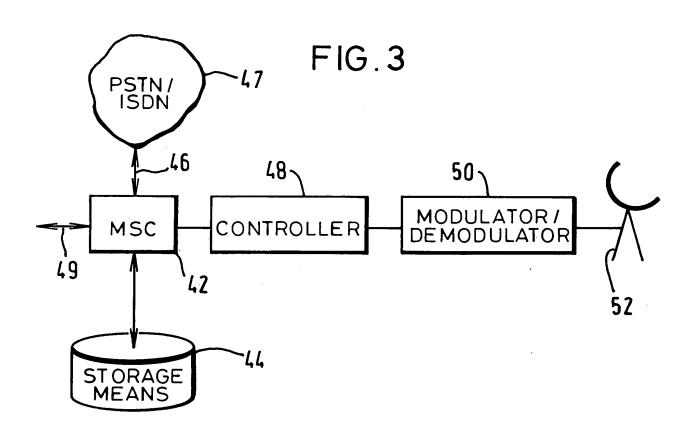
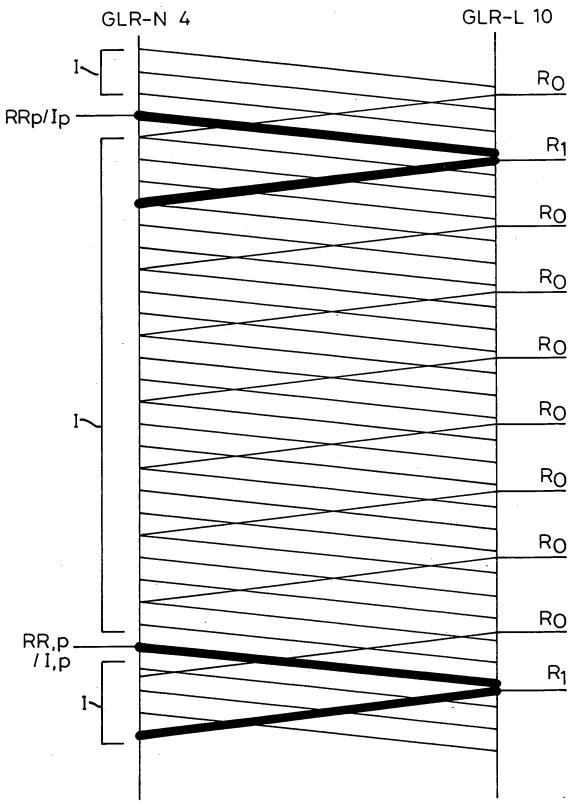


FIG. 2









No.	1 2 3 4 5 6 7 8 SPARE V N(R)	SPARE V N(R)	SPARE V i
CONTROL INFORMATION 16 BITS 48 BITS	1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 1 1 1 1 N(R)	FIG. 5	

FIG.6

